UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/601,643	06/24/2003	Mutsuko Hatano	NITT.0142	1270

38327 7590 02/21/2007

REED SMITH LLP
3110 FAIRVIEW PARK DRIVE, SUITE 1400
FALLS CHURCH, VA 22042

EXAMINER	
MOON, SEOKYUN	
ART UNIT	PAPER NUMBER
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/601,643	HATANO ET AL.	
	Examiner	Art Unit	
	Seokyun Moon	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10 and 11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10 and 11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. The Applicants' arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1-8** and **11** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaise et al. (US 6,483,495, herein after "Kaise") and Applicants Admitted Prior Art (herein after, "AAPA"), and further in view of Yamada (US 2002/0158298).

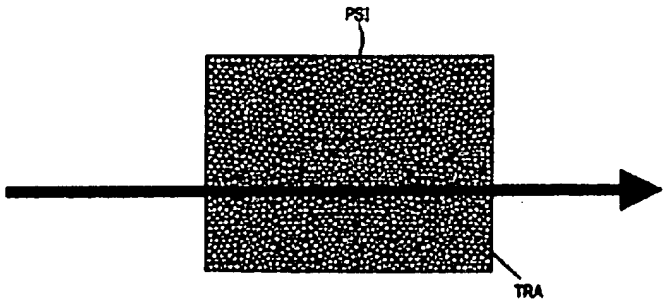
As to **claim 1**, Kaise [fig. 1a] teaches an image display device ("active matrix type liquid crystal display device 100") having an active matrix substrate ("base substrate 110") provided with a pixel region ("display region 140") [col. 6 lines 1-8] having a plurality of pixels arranged in a matrix configuration [fig. 2a], and a drive circuit region ("drive circuitry region 150") disposed outside of said pixel region [col. 6 lines 9-10] for supplying drive signals to the plurality of pixels via interconnection lines ("scanning lines 112" and "data signal lines 113") [fig. 2b] [col. 6 lines 58-61],

wherein: the driver circuit region ("drive circuitry region 150") [fig. 2a] comprises a plurality of stages of circuit sections ("shift register circuit 131", "buffer circuit 132", and "sample holding circuit 133") successively processing an externally supplied display

signal (the signal inputted to the "shift register circuit 131") to produce a drive signal (the signal outputted from the "sample holding circuit 133") to be supplied to the pixel region ("display region 140"), each of the plurality of stages of circuit sections having a different function [col. 7 lines 50-67], at least one of the plurality of stages of circuit sections ("shift register circuit 131", "buffer circuit 132", and "sample holding circuit 133") is provided with active elements [col. 7 lines 60-62].

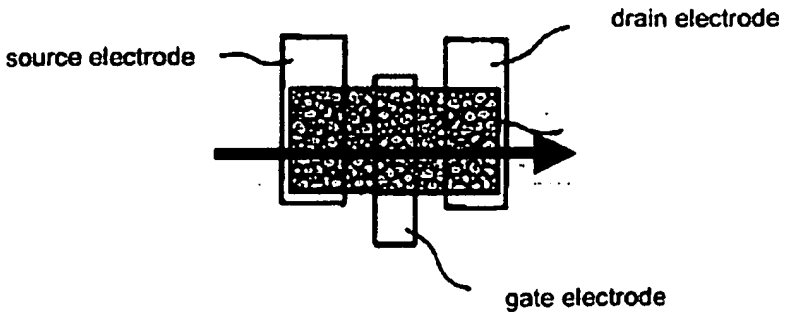
Kaise does not expressly teach the active elements being fabricated in discontinuous converted regions formed of roughly-band-shaped-crystal silicon films having grain boundaries continuous in generally one direction and having a direction of movement of carriers therein a direction of the grain boundaries.

However, AAPA discloses active elements being fabricated in discontinuous (the converted polysilicon film PSI has boundaries to be implemented in a limited size of a display, thus requires to be discontinuous at the boundaries) converted (converted from an "amorphous silicon film ASI" into a "polysilicon film PSI" by irradiating excimer laser light ELA on the "amorphous silicon film ASI") regions ("polysilicon film PSI") [appl. pg 3 line 13 - pg 4 line 25] formed of roughly-band-shaped-crystal silicon films [appl. fig. 35b: "PSI-L"] having grain boundaries continuous in generally one direction [drawing 1 provided below, which is equivalent to Appl. fig. 35a] [appl. pg 4 lines 18-21],



Drawing 1

and the active elements ("TFT") to have a direction of movement of carriers (electrons or holes) therein in a direction of grain boundaries [drawing 2 provided below, which is equivalent to Appl. fig. 35b, wherein it is inherent that electrons moves from source to drain in a transistor].



Drawing 2

It would have been obvious to one of ordinary skill in the art at the time of the invention to fabricate Kaise's active elements included in a plurality of stages of drive circuit sections on polysilicon films in a way as taught by AAPA, in order to provide the active elements with high mobility, thus to provide an image with better quality [appl. pg 2 lines 8-17].

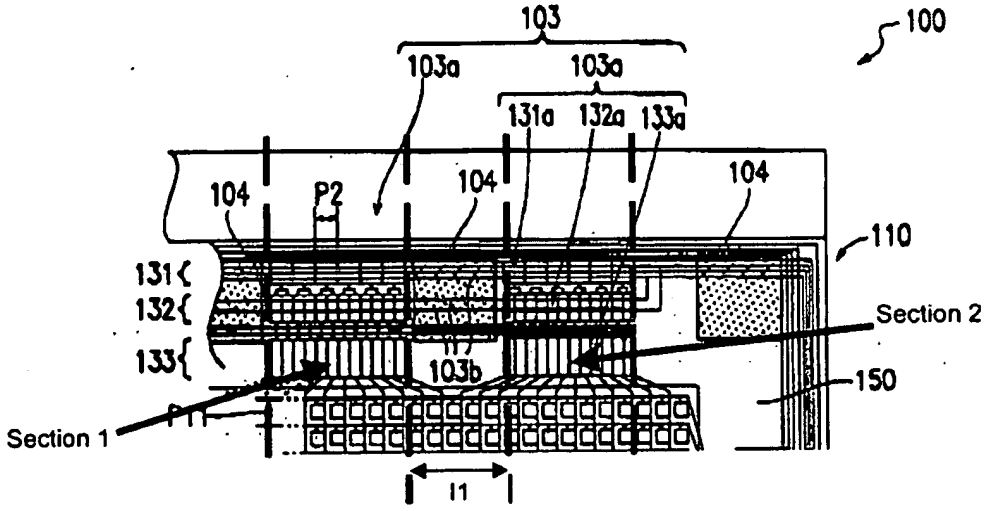
Kaise modified by AAPA does not expressly disclose the active elements in the pixel region and the active elements in the drive circuit region being formed of a portion of a polysilicon film which are formed over a substantially entire area of a substrate of the image display device.

However, Yamada teaches an idea of forming transistors (i.e. active elements) included in a driver section and in a pixel section on a same substrate of a display using polycrystalline silicon as an active layer [par. (0022)].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kaise's device to form the active elements of a pixel section and the active elements of a driver section on a single substrate using polycrystalline silicon as

an active layer, as taught by Yamada, in order to reduce space required to implement active elements within a display, thus to save the space within a display, efficiently [par. (0024)].

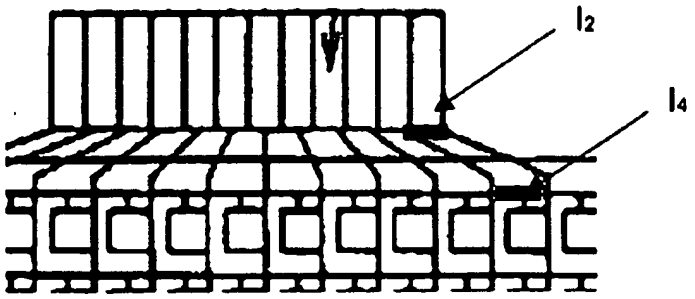
As to **claim 2**, Kaise [fig. 2a] teaches that the circuit sections ("section 1" and "section 2" shown on drawing 3 of this office action, which is equivalent to fig. 2a) of each of the plurality of stages ("shift register circuit 131", "buffer circuit 132", and "sample holding circuit 133") are arranged along one side (upper side) of the active matrix substrate ("base substrate 110") at specified intervals ("11" shown in drawing 3) at a periphery thereof.



Drawing 3

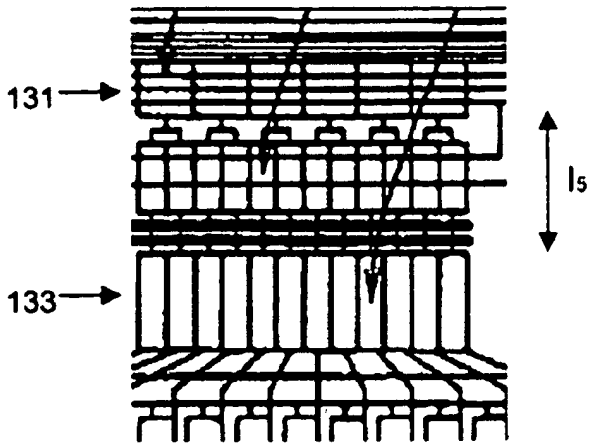
As to **claim 3**, Kaise [fig. 2a] teaches that circuit sections ("sample holding circuit 133") having the active elements formed therein are in a final output stage of the plurality of stages ("shift register circuit 131", "buffer circuit 132", and "sample holding circuit 133") [col. 7 lines 60-62], and

the interconnection lines coupling the final output stage to the plurality of pixels are arranged at wider intervals on a pixel-region side thereof than a final-output- stage side thereof [drawing 4 provided below, which is equivalent to fig. 2a: $l_2 < l_4$].



Drawing 4

As to **claim 4**, Kaise [fig. 2A] teaches that the circuit sections ("shift register circuit 131" and "sample holding circuit 133") having the active elements formed therein are arranged in two or more parallel rows along one side of the active matrix substrate at specified intervals ("l_5") at a periphery thereof [drawing 5 provided below, which is equivalent to fig. 2a] [col. 2 lines 64-67].



Drawing 5

As to **claim 5**, Kaise [fig. 1B] teaches said active elements (the switching elements included in the "sample holding circuit 133" which is included in "data driver

103") [col. 7 lines 51-54 and lines 60-62] being arranged along two opposed sides of said active matrix substrate ("base substrate 110") at specified intervals ("h") at peripheries thereof [drawing 3 provided on page 5 of this Office Action].

As to **claim 6**, Kaise as modified by AAPA and Yamada does not expressly disclose that areas of the circuit sections having the active elements formed therein vary with a scale thereof.

However, Examiner takes official notice that it is well known in the art at the time of the invention to increase the size of the circuit sections included in the driving circuitry of a display to provide driving signals for greater number of pixels when the size of the display is increased.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the areas of the combined circuit section of Kaise as modified by AAPA and Yamada occupied in a display to vary with a scale to accommodate the change on the number of pixels to drive when the size of the display changes.

As to **claim 7**, all of the claim limitations have already been discussed with respect to the rejection of claim 4 except for the circuit sections in one of the two or more rows being offset in longitudinal directions.

Kaise [fig. 2a] teaches that the circuit sections ("sample holding circuit 133") in one of the two or more rows ("shift register circuit 131" and "sample holding circuit 133") are offset in longitudinal directions thereof from the circuit sections in an adjacent one of the two or more rows.

As to **claim 8**, all of the claim limitations have already been discussed with respect to the rejection of claim 7 since the active elements are included in the circuit sections.

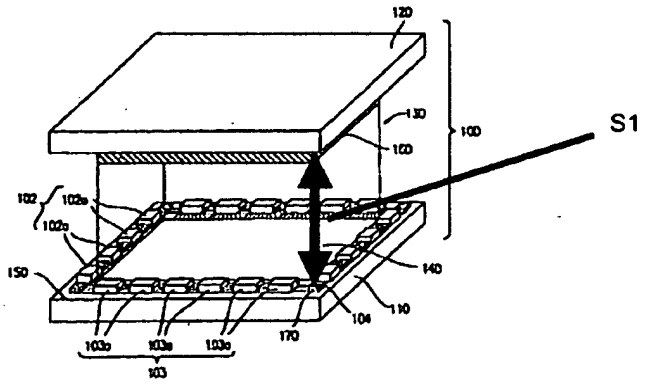
As to **claim 11**, Kaise does not teach each of the pixels to comprise an organic EL layer.

However, examiner takes official notice that specifying each of plural pixels included in a display to comprise an organic EL layer is well known in the art.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use Kaise's method of optimizing driving circuitry in the driving circuitry for EL displays, to prevent a reduction of image quality for the display and to provide a method of miniaturizing the display [col. 5 lines 12-22] since Kaise provides a method of preventing a threshold fluctuation of an active element included in the drive circuitry and EL displays include a plurality of active elements.

4. **Claim 10** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kaise, AAPA, Yamada as applied to claims 1-8 and 11 above, and further in view of Nagata et al. (US 6,118,505, herein after "Nagata").

Kaise [fig. 1a] teaches an image display device ("liquid crystal display device 100") comprising a liquid crystal layer ("130"), wherein the liquid crystal layer is sandwiched between the active matrix substrate ("base substrate 110") and a counter substrate ("120") superposed on the active matrix substrate with a specified spacing ("S1" shown in drawing 6, which is equivalent to fig. 1a) therebetween.



Drawing 6

Kaise does not expressly disclose having a color filter substrate.

However, Nagata teaches a liquid crystal display device having a color filter being formed in the counter substrate [col. 17 lines 65-67].

It would have been obvious to one of ordinary skill in the art at the time of the invention to include Nagata's color filter in Kaise's counter substrate to produce adequate colors for each of plural pixels and thus to provide adequate colors for the images to be displayed on the display.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Seokyun Moon whose telephone number is (571) 272-5552. The examiner can normally be reached on Mon - Fri (8:30 a.m. - 5:00 p.m.).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

February 9, 2007 – s.m.

SUMATI LEFKOWITZ
SUPERVISORY PATENT EXAMINER